

AMENDMENT

Serial Number: 10/023,819

Filing Date: December 21, 2001

Title: CHIP JOIN PROCESS TO REDUCE ELONGATION MISMATCH BETWEEN THE ADHERENTS AND SEMICONDUCTOR PACKAGE MADE THEREBY

Assignee: Intel Corporation

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IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method of soldering a coefficient of thermal expansion mismatched semiconductor chip and substrate to one another, the method comprising:
thermally expanding each of the semiconductor chip and the substrate substantially a
[[the]] same amount in a direction along surfaces thereof to be joined by soldering; and
soldering the thermally expanded semiconductor chip and the substrate to one another.
2. (Currently Amended) The method according to claim 1, wherein the thermally expanding includes heating the semiconductor chip to at least a soldering temperature for soldering the chip and the substrate.
3. (Currently Amended) The method according to claim 1, wherein the thermally expanding comprises separately heating the chip and the substrate to different temperatures as a function of the mismatch of their coefficients of thermal expansion and thereafter assembling the chip and the substrate in contact with one another for the soldering.
4. (Currently Amended) The method according to claim 1, wherein the soldering includes assembling the thermally expanded semiconductor chip and the substrate in contact with one another via a solder to form a soldered assembly, and wherein the method further comprises cooling the soldered assembly to room temperature.

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5. (Original) The method according to claim 1, further comprising applying a solder to the semiconductor chip prior to thermally expanding the chip, and wherein the soldering includes contacting the solder on the thermally expanded chip with the substrate to wet the substrate and form at least one soldered joint.

6. (Currently Amended) The method according to claim 1, wherein the substrate comprises a plurality of standoff elements upstanding from a surface of the substrate, and wherein the soldering includes forming a plurality of soldered joints connecting the thermally expanded semiconductor chip to [[the]] tops of respective ones of the standoff elements on the thermally expanded substrate.

7. (Currently Amended) The method according to claim 6, wherein the standoff elements are non-melting at a [[the]] soldering temperature.

8. (Original) The method according to claim 1, wherein the soldering includes simultaneously forming a plurality of soldered joints between the semiconductor chip and the substrate.

9. (Currently Amended) The method according to claim 1, wherein the soldering includes making a plurality of soldered joints between the chip and the substrate along the chip over a

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distance of at least 4 mm from a ~~for the~~ center of the chip.

10. (Currently Amended) A method of joining first and second coefficient of thermal expansion mismatched members to one another, the method comprising:

thermally expanding each of the first and second members substantially a ~~[[the]]~~ same amount in a direction along surfaces thereof to be joined;

joining the thermally expanded first and second members to one another at an elevated temperature; and

cooling the joined first and second members to room temperature.

11. (Currently Amended) The method according to claim 10, wherein the thermally expanding includes heating a ~~[[the]]~~ member of the first and second members having a ~~the~~ lower coefficient of thermal expansion to at least the elevated temperature at which the joining takes place.

12. (Original) The method according to claim 10, wherein the thermally expanding comprises separately heating each of the first and second members to respective temperatures as a function of the mismatch of their coefficients of thermal expansion and thereafter assembling the members in contact with one another for the joining.

13. (Currently Amended) The method according to claim 10, wherein the joining at the

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[[an]] elevated temperature is by soldering.

14. (Currently Amended) An electronic assembly comprising:

a substrate having a first coefficient of thermal expansion;

a semiconductor chip having a second coefficient of thermal expansion which is different than the first coefficient of thermal expansion;

a plurality of soldered joints connecting the semiconductor chip and the substrate;

wherein the chip and the substrate across the plurality of ~~respective~~ soldered joints of the electronic assembly at room temperature have coefficient of thermal expansion difference induced elongation mismatches and stresses induced thereby in the electronic assembly from soldering; and

wherein a ~~[[the]]~~ magnitude of the elongation mismatches and the stresses induced thereby in the electronic assembly ~~is~~are less than one-half that expected based upon cooling the substrate and the semiconductor chip from a ~~[[the]]~~ solder solidification temperature to the room temperature following soldering of the plurality of soldered joints.

15. (Currently Amended) The electronic assembly according to claim 14, wherein the elongation mismatches and the stresses induced thereby in the electronic assembly are reflected in the electronic assembly by at least one of post-soldering ~~post-soldering~~ residual stress, residual plastic deformation in the plurality of soldered joints, residual plastic deformation in the substrate, and semiconductor chip warpage.

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16. (Original) The electronic assembly according to claim 14, wherein the first coefficient of thermal expansion of the substrate is more than two times greater than the second coefficient of thermal expansion of the semiconductor chip.

17. (Currently Amended) An electronic assembly comprising:

a substrate having a first coefficient of thermal expansion;

a semiconductor chip having a second coefficient of thermal expansion which is different than the first coefficient of thermal expansion;

a plurality of soldered joints connecting the semiconductor chip and the substrate;

wherein the chip and the substrate across the plurality of ~~respective~~ soldered joints of the electronic assembly at room temperature have coefficient of thermal expansion difference induced elongation mismatches from soldering; and

wherein a ~~[[the]]~~ magnitude of the elongation mismatches is ~~[[are]]~~ less than one-half that expected based upon cooling the substrate ~~substate~~ and the semiconductor chip from a ~~[[the]]~~ solder solidification temperature to the room temperature following soldering of the plurality of soldered joints; and

wherein the substrate comprises a plurality of standoff elements upstanding from a surface of the substrate, and wherein the plurality of soldered joints connect the semiconductor chip to ~~[[the]]~~ tops of respective ones of the plurality of standoff elements.

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18. (Currently Amended) The electronic assembly according to claim 17, wherein the standoff elements are non-melting at a ~~[[the]]~~ solder liquidous temperature.

19. (Currently Amended) The electronic assembly according to claim 17, wherein the plurality of standoff elements are copper bumps.

20. (Currently Amended) The electronic assembly according to claim 14, wherein the semiconductor chip is joined by the plurality of soldered joints to the substrate along the chip over a distance of at least 4 mm from a ~~[[the]]~~ center of the chip.

21. (Currently Amended) The electronic assembly according to claim 14, wherein the plurality of soldered joints each comprise solder on the semiconductor chip that ~~which~~ is wetted onto a surface of the substrate to form the soldered joint.

22. (Currently Amended) A semiconductor package comprising:

a package substrate having a first coefficient of thermal expansion of at least 15 ppm/°C,
the package substrate having a plurality of contact members;

a semiconductor chip having a coefficient of thermal expansion which is at least 2.7
ppm/°C less than the coefficient of thermal expansion of the package substrate, a front side of the
chip having a plurality of solder connections thereon, the semiconductor chip being located on
the substrate with plurality of the solder connections connected to respective ones of the plurality

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of contact members by soldered joints electrically coupling the semiconductor chip to the package substrate;

wherein the semiconductor chip and the package substrate across the respective soldered joints of the semiconductor package at room temperature have coefficient of thermal expansion difference induced elongation mismatches and stresses induced thereby in the semiconductor package from soldering; and

wherein a ~~[[the]]~~ magnitude of the elongation mismatches and the stresses induced thereby in the semiconductor package ~~is~~are less than one-half that expected based upon cooling the substrate and the semiconductor chip from a ~~[[the]]~~ solder solidification temperature to the room temperature following the soldering of the soldered joints.

23. (Currently Amended) The semiconductor package according to claim 22, wherein the elongation mismatches and the stresses induced thereby in the semiconductor package are reflected in the semiconductor package by at least one of post-soldering ~~post-soldering~~ residual stress, residual plastic deformation in the soldered joints, residual plastic deformation in the substrate, and semiconductor chip warpage.

24. (Original) The semiconductor package according to claim 22, wherein the first coefficient of thermal expansion of the substrate is more than two times greater than the second coefficient of thermal expansion of the semiconductor chip.

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25. (Currently Amended) A semiconductor package comprising:

a package substrate having a first coefficient of thermal expansion of at least 15 ppm/°C,
the package substrate having a plurality of contact members;

a semiconductor chip having a coefficient of thermal expansion which is at least 2.7
ppm/°C less than the coefficient of thermal expansion of the package substrate, a front side of the
chip having a plurality of solder connections thereon, the semiconductor chip being located on
the substrate with the plurality of solder connections connected to respective ones of the plurality
of contact members by soldered joints electrically coupling the semiconductor chip to the
package substrate;

wherein the semiconductor chip and the package substrate across the respective soldered
joints of the semiconductor package at room temperature have coefficient of thermal expansion
difference induced elongation mismatches from soldering; and

wherein a ~~[[the]]~~ magnitude of the elongation mismatches is ~~[[are]]~~ less than one-half that
expected based upon cooling the substrate and the semiconductor chip from a ~~[[the]]~~ solder
solidification temperature to a room temperature following the soldering of the soldered joints;
and

wherein the plurality of contact members comprise a plurality of standoff elements
upstanding from a surface of the substrate, and wherein the soldered joints connect the
semiconductor chip to ~~[[the]]~~ tops of respective ones of the plurality of standoff elements.

26. (Currently Amended) The semiconductor package according to claim 25, wherein the

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plurality of standoff elements are non-melting at a a ~~[[the]]~~ solder liquidous temperature.

27. (Currently Amended) The semiconductor package according to claim 25, wherein the plurality of standoff elements are copper bumps.

28. (Currently Amended) The semiconductor package according to claim 22, wherein the semiconductor chip is joined by soldered joints to the substrate along the chip over a distance of at least 4 mm from a ~~[[the]]~~ center of the chip.

29. (Currently Amended) The semiconductor package according to claim 22, wherein the soldered joints each comprise solder on the semiconductor chip that ~~which~~ is wetted onto a surface of a contact member of the substrate to form a ~~[[the]]~~ soldered joint.